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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,799	01/18/2002	Seung Won Seo	2598/OK192	3199

7590 11/04/2005

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EXAMINER	
DESIR, JEAN WICEL	
ART UNIT	PAPER NUMBER
2614	

DATE MAILED: 11/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,799	SEO ET AL.	
	Examiner	Art Unit	
	Jean W. Désir	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *39-43* is/are allowed.

6)☒ Claim(s) *1-5,8,10,12-15,19,21-24,28,30-33,37 and 44-50* is/are rejected.

7)☒ Claim(s) *6,7,9,11,16-18,20,25-27,29,34-36 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/18/02
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 44-50, 1-5, 8, 10, 12-15, 19, 21-24, 28, 30-33, 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Moon et al (US 6,437,522).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Claim 44:

Moon discloses:

"A convergence error correcting apparatus (see col. 5 lines 38-48, Fig. 14) in a display device, comprising a memory (see Fig. 14 items 13C, 13D, col. 20 lines 37-60, col. 21 lines 10-25) storing a plurality of independent and separate convergence error

correction data signals corresponding to respective correction points within a period of a specific horizontal synchronization signal".

Claim 45:

Moon discloses:

"A convergence error correcting apparatus (see col. 5 lines 38-48, Fig. 14) in a display device, comprising a memory (see Fig. 14 items 13C, 13D, col. 20 lines 37-60, col. 21 lines 10-25) storing a plurality of independent and separate convergence error correction data signals corresponding to respective correction points within each period of specific horizontal synchronization signals, said memory storing a plurality of interpolation data signals (col. 20 lines 37-60, col. 21 lines 10-25) corresponding to horizontal synchronization signals disposed between adjacent correction points".

Claim 46:

Moon discloses:

"A convergence error correcting apparatus (see Figs. 10, 14) in a display device, comprising a controller (see col. 5 lines 38-48, col. 20 lines 32-60) independently and separately generating a plurality of independent and separate convergence error correction data signals corresponding to respective correction points of a screen pattern and independently and separately applying each of convergence error correction data signals to magnetic field controlling coils (see outputs of Fig. 14) when each correction point corresponding to respective convergence error correction data signals is scanned in a screen".

Claim 47:

Moon discloses:

A convergence error correcting apparatus (see Figs. 10, 14) in a display device, comprising: a memory (see Fig. 14 items 13C, 13D, col. 20 lines 37-60, col. 21 lines 10-25) storing a plurality of independent and separate convergence error correction data signals corresponding to respective correction points within each period of specific horizontal synchronization signals, said memory storing a plurality of interpolation data signals (col. 20 lines 37-60, col. 21 lines 10-25) corresponding to horizontal synchronization signals disposed between adjacent correction points; and a controller (see Fig. 14 items 11, col. 20 lines 32-60, col. 5 lines 38-48) coupled to said memory, independently reading each of said convergence error correction data signals from said memory when corresponding correction point is scanned in a screen.

Claim 48:

Moon discloses:

A convergence error correcting apparatus (see Figs. 10, 14) in a display device, comprising a controller (see col. 5 lines 38-48, col. 20 lines 32-60) generating a first separate and independent convergence error correction data corresponding to respective first pixels in a first screen having a first screen size in response to the number of first horizontal synchronization signals in a first vertical synchronization signal, said controller generating a first separate and independent interpolation data signals (col. 20 lines 32-60, col. 21 lines 10-25) corresponding to a first area disposed between adjacent first pixels, said controller generating a second separate and independent convergence correction data (col. 20 lines 37-60, col. 21 lines 10-25)

corresponding to respective second pixels in a second screen having a second screen size in response to the number of second horizontal synchronization signals in a second vertical synchronization signal, said controller generating a second separate and independent interpolation data signals (col. 20 lines 37-60, col. 21 lines 10-49) corresponding to a second area disposed between adjacent second pixels.

Claim 49 is rejected for the same reasons as claims 45, 46.

Claim 50:

Moon discloses:

A process in a convergence error correcting apparatus (see Figs. 10, 14), comprising the steps of:

storing (see Fig. 14 item 13C, col. 20 lines 37-60, col. 21 lines 10-25) a first separate and independent convergence error correction data corresponding to respective first pixels in a first screen having a first screen size in response to the number of first horizontal synchronization signals in a first vertical synchronization signal;

storing (see Fig. 14 item 13D, col. 20 lines 37-60, col. 21 lines 10-25) a first separate and independent interpolation data signals corresponding to a first area disposed between adjacent first pixels;

converting (see Fig. 14 items 21-25, 17-19, col. 20 lines 37-60, col. 21 lines 10-49) said first convergence error correction data signals and said first interpolation data signals into a second separate and independent convergence correction data and a second interpolation data signals corresponding to respective second pixels in a second

screen signal having a second screen size in response to the number of second horizontal synchronization signals in a second vertical synchronization signal.

Claim 1:

Moon discloses:

A digital dynamic convergence error control system (see Figs. 10, 12, 14) comprising:

a convergence error detecting apparatus recognizing crossing points of a screen pattern displayed on a screen of a display device, detecting each amount of convergence errors corresponding to respective crossing points (col. 17 line 56 to col. 18 line 32);

a main control means generating correction data in response to respective convergence errors, generating interpolation data using said correction data of adjacent crossing points (see col. 20 lines 32-60);

and a digital dynamic convergence error control apparatus receiving said correction data and said interpolation data from said main control means, storing said correction data and said interpolation data in a memory (see col. 21 lines 10-26, col. 20 lines 37-60), converting each of said correction data and said interpolation data into voltage or current in response to respective horizontal synchronization signals extracted from a picture signal, and independently and separately applying said voltage or said current to a magnetic field controlling coil only during a corresponding period of respective horizontal synchronization signals (see Fig. 14 items 21-25, 17-19, col. 5 lines 38-48, col. 21 lines 10-49).

Claim 2 is inherent to Moon's disclosure.

Claim 3 is disclosed, see Fig. 11, col. 17 line 56 to col. 18 line 32.

Claim 4 is disclosed, see col. 20 lines 32-51, Fig. 11.

Claim 5 is disclosed: a controller as claimed, see Figs. 12, 14 item 11, col. 20 lines 32-62; a reference clock generator as claimed, see Figs. 12, 14 items 14, 11; an address generator as claimed, see Fig. 14 item 16, col. 20 lines 32-60, col. 21 lines 10-50; an internal memory as claimed, see Fig. 14 items 13C, 13D; and an output section as claimed, see Fig. 14 items 21-25, 17-19, col. 5 lines 38-48, col. 21 lines 10-49.

Claim 8 is disclosed, see Fig. 14 item 13A.

Claim 10 is disclosed, see outputs of Fig. 14 and items 17-19.

Claim 12 is rejected for the same reasons as claim 5, because nonvolatile external memory as claimed is also disclosed (See Fig. 14 item 13A).

Claims 13-15 are for the same reasons as claims 2-4.

Claim 19 is rejected for the same reasons as claim 10.

Claim 21 is rejected for the same reasons as claim 12, because coil separator, horizontal deflection, vertical deflection, and a plurality of magnetic field, as claimed, are also disclosed (see outputs of Fig. 14, Fig. 15, col. 22 lines 23-51).

Claims 22-24 are for the same reasons as claims 13-15.

Claim 28 is rejected for the same reasons as claim 19.

Claim 30 is rejected for the same reasons as claim 21.

Claims 31-33 are for the same reasons as claims 22-24.

Claim 37 is rejected for the same reasons as claim 28.

Allowable Subject Matter

3. Claims 6, 7, 9, 11, 16, 17, 18, 20, 25, 26, 27, 29, 34, 35, 36, 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims **39**, 40, **41**-43 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean W. Désir whose telephone number is (571) 272 7344. The examiner can normally be reached on 5/4/9 - First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W. Miller can be reached on (571) 272 7353. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JWD
Oct. 26, 05

JOHN MILLER
SUPERVISORY PATENT EXAMINER
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